

FIG. 1

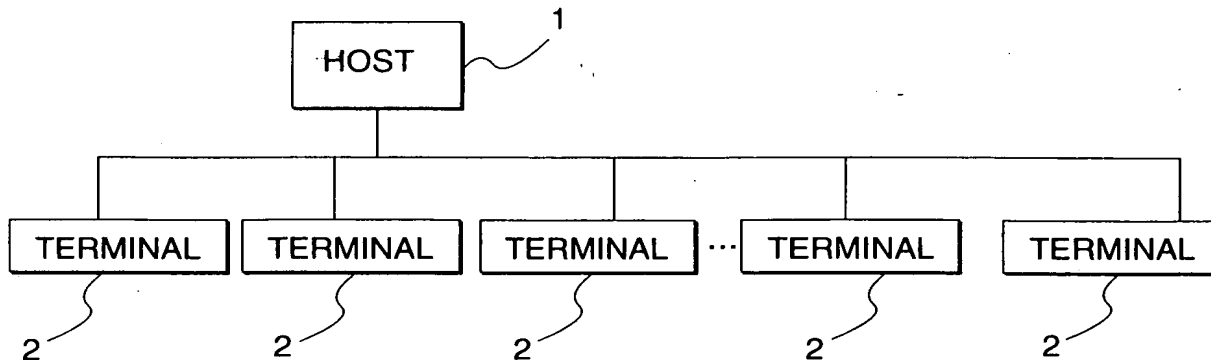


FIG. 2

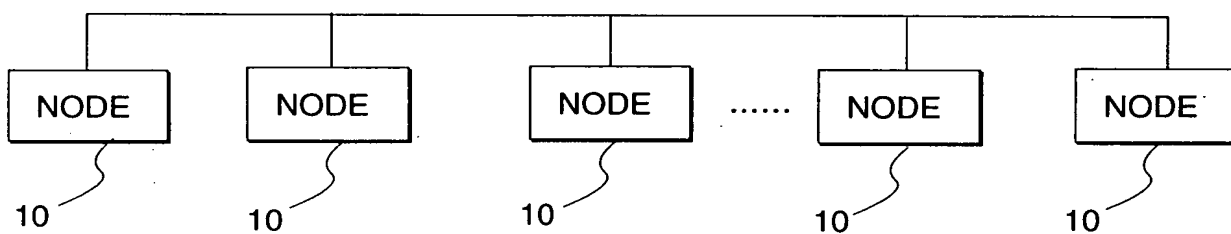


FIG. 3

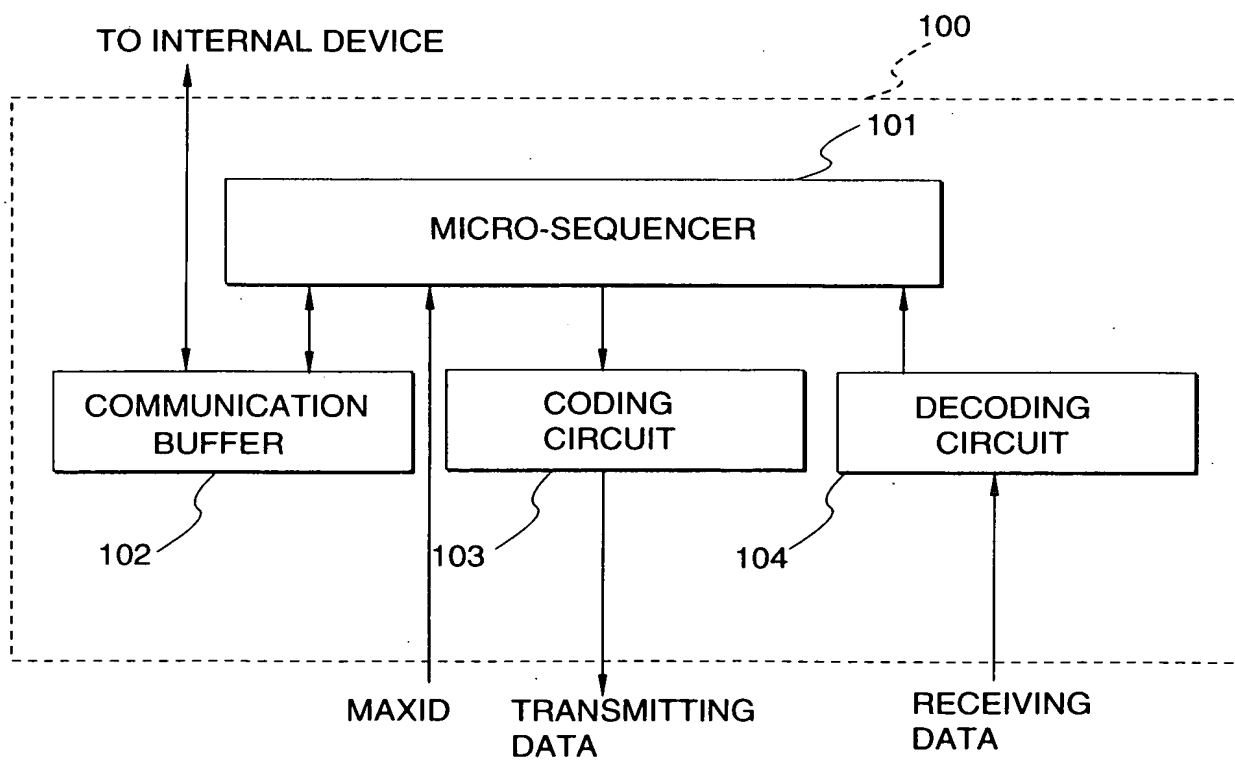


FIG. 4

ALERT	SID	DID	DID	CP	DATA 0	DATA 1		DATA N	CRC	CRC
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FIG. 5

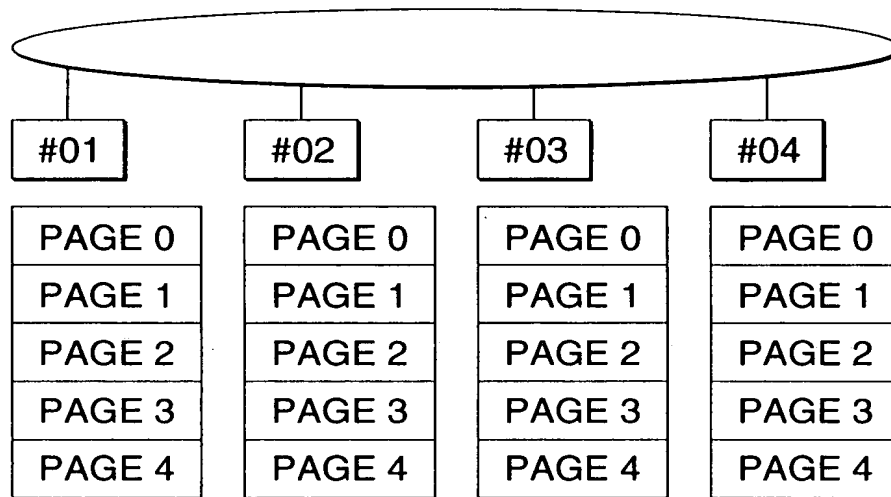


FIG. 6

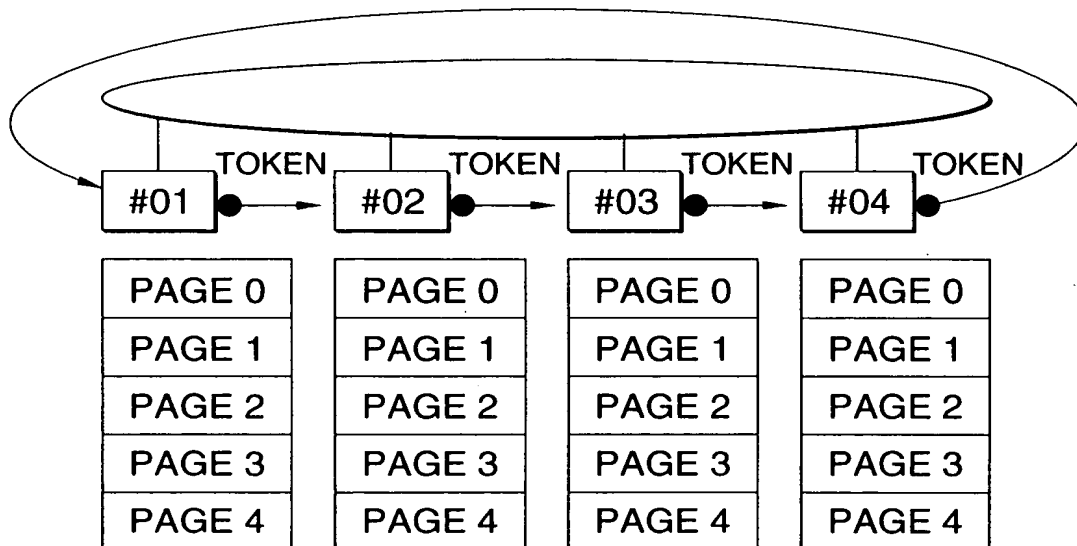


FIG. 7

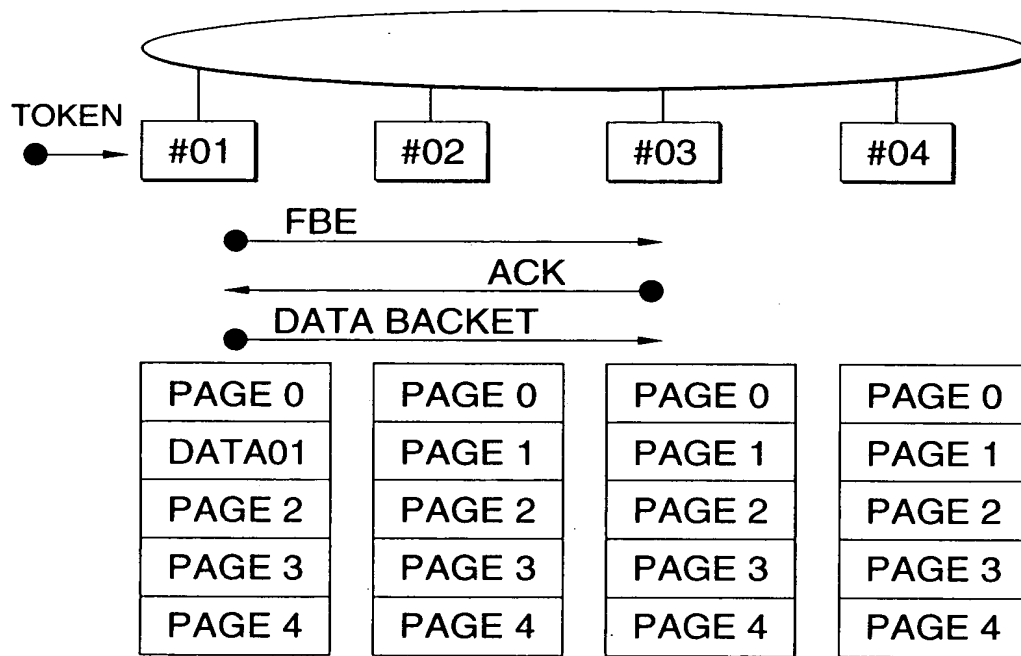


FIG. 8

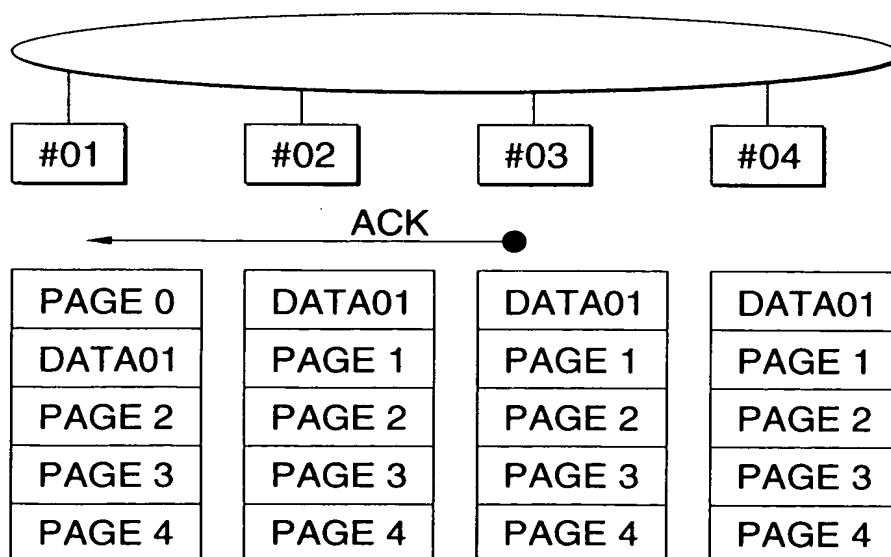


FIG. 9

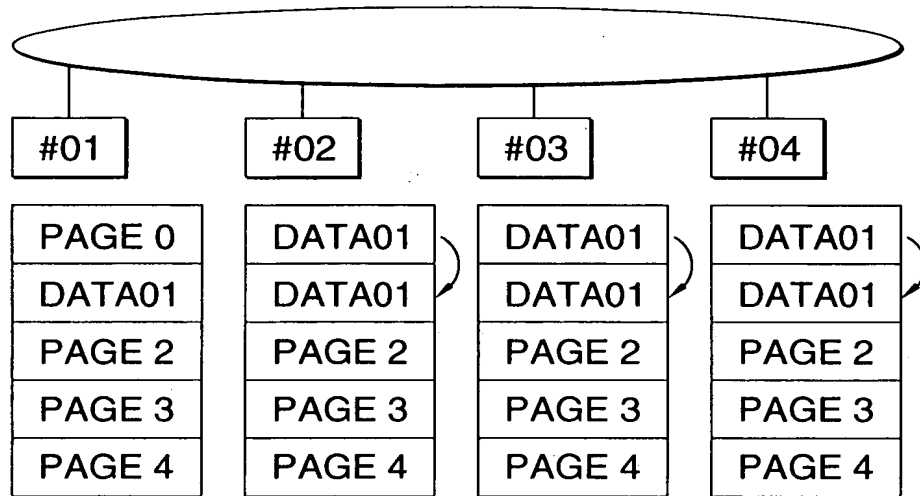


FIG. 10

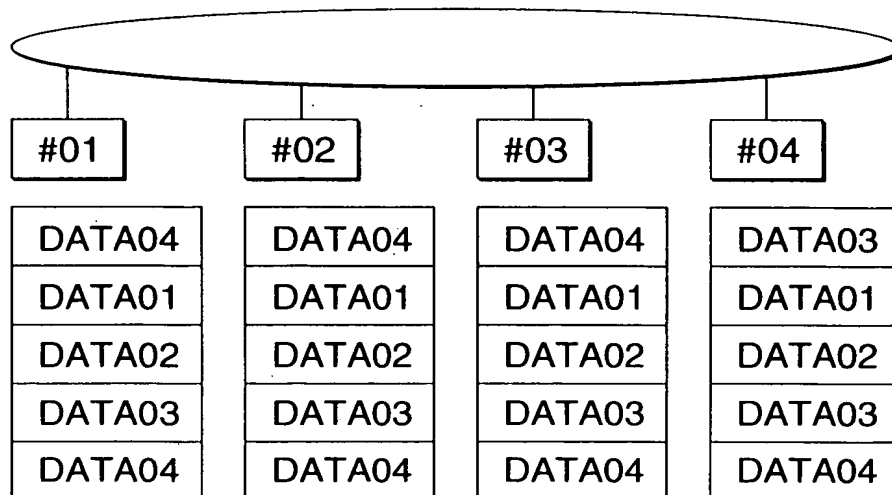


FIG. 11

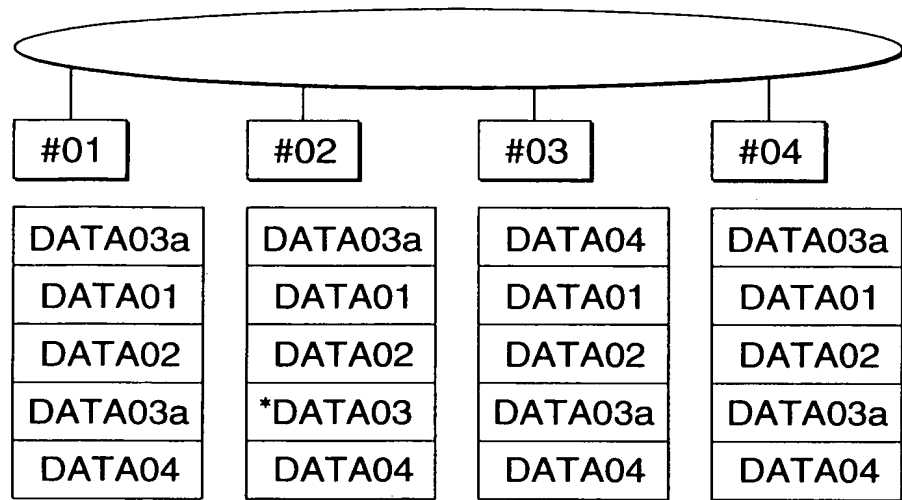


FIG. 12

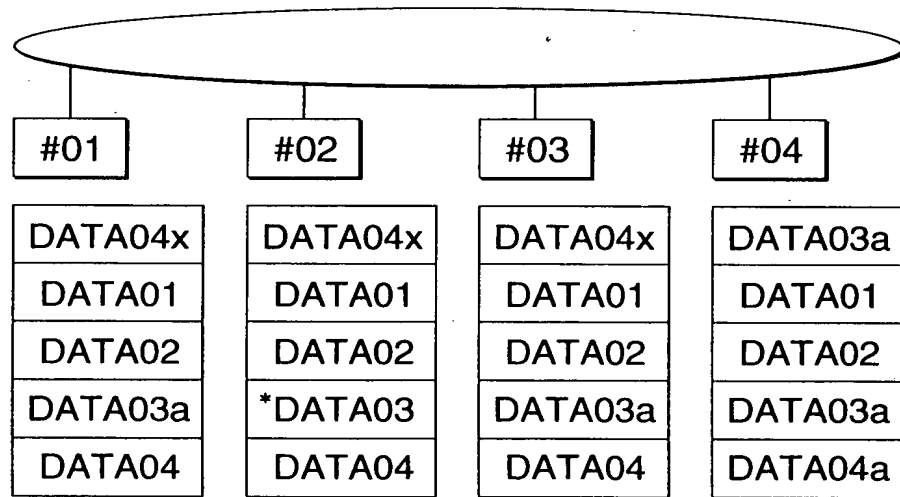


FIG. 13

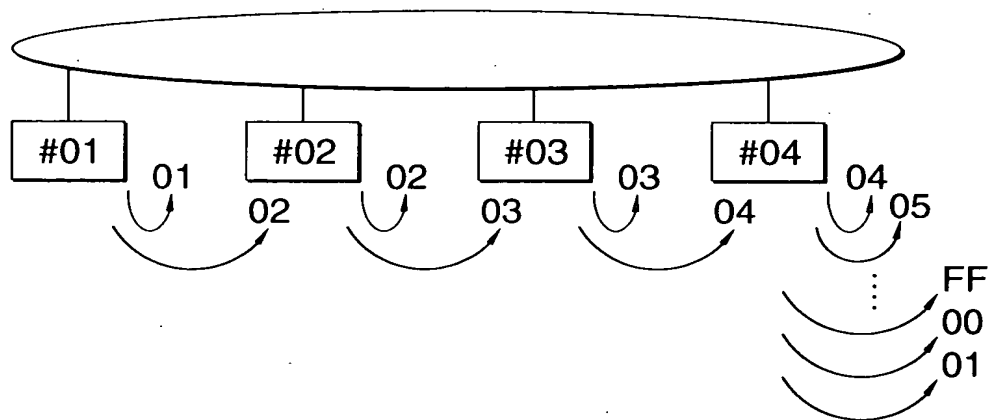


FIG. 14

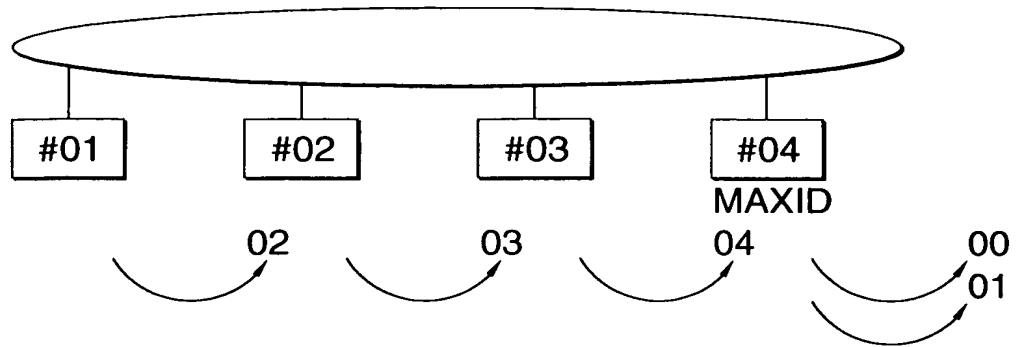


FIG. 15

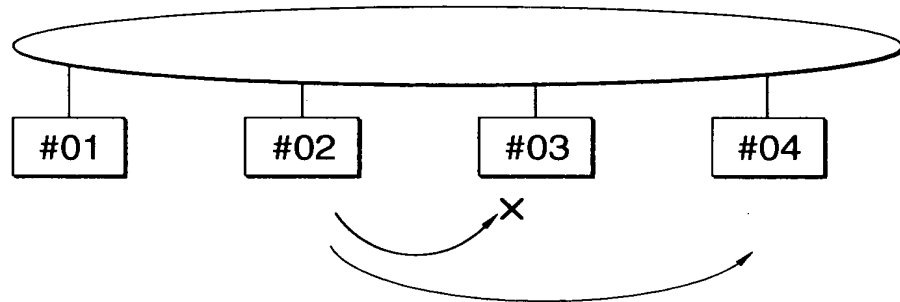


FIG. 16

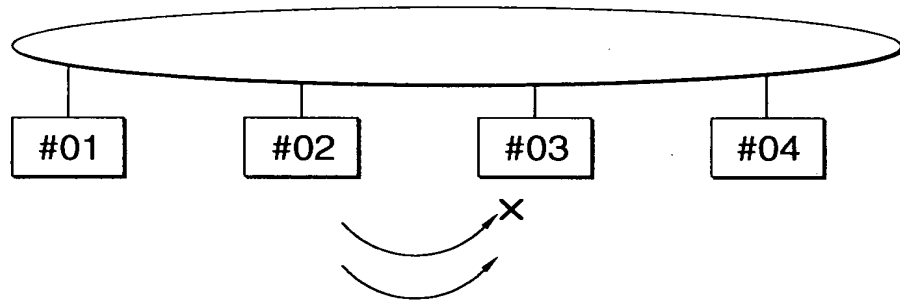
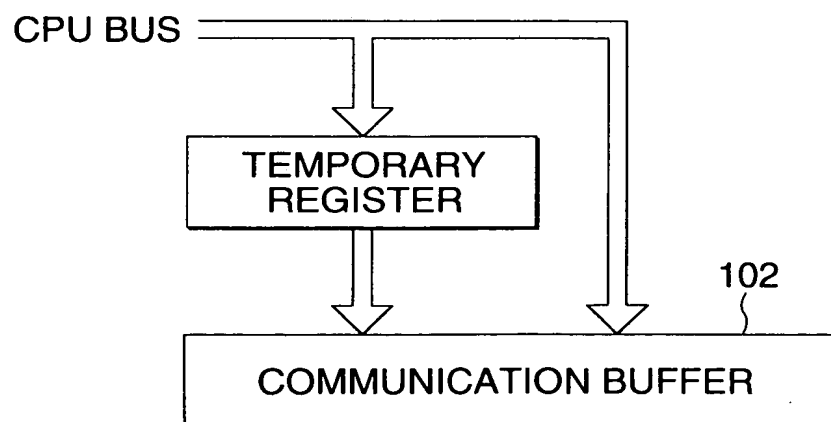


FIG. 17







The diagram shows a system 100 enclosed in a dashed box. At the top is the **I/O PORT** 101, which has a bidirectional arrow connecting it to the **MICRO-SEQUENCER** block below it. The **MICRO-SEQUENCER** is a central rectangular block. Below it are three other blocks: **COMMUNICATION BUFFER** 102 on the left, **CODING CIRCUIT** 103 in the middle, and **DECODING CIRCUIT** 104 on the right. Bidirectional arrows connect the **MICRO-SEQUENCER** to each of these three blocks. The **COMMUNICATION BUFFER** 102 has a bidirectional arrow extending upwards from the top of the dashed box, labeled **TO INTERNAL DEVICE**. The **CODING CIRCUIT** 103 has a downward arrow from its bottom extending below the dashed box, labeled **TRANSMITTING DATA**. The **DECODING CIRCUIT** 104 has an upward arrow from below the dashed box, labeled **RECEIVING DATA**, pointing into its bottom.

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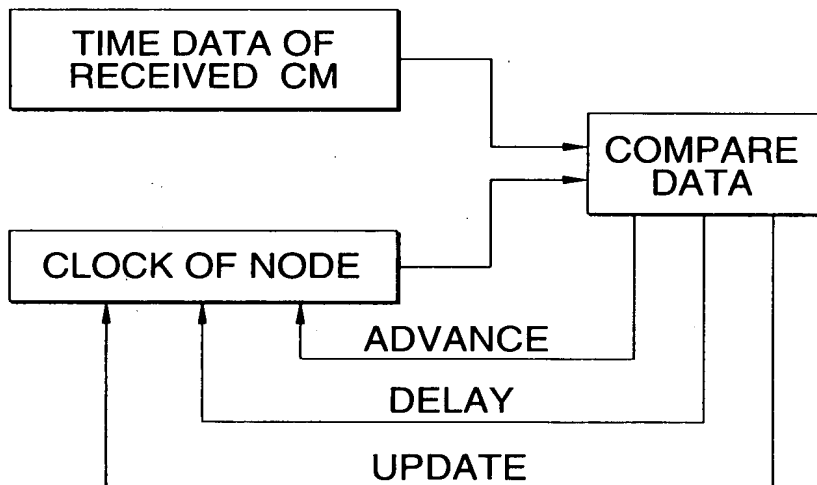
graph LR
    subgraph 1001 [TRANSMISSION BUFFER]
        direction TB
        HP[HEADER PART]
        DP[DATA PART]
        RTD[REPLACED WITH TIME DATA]
    end
    subgraph 1002 [CLOCK]
        direction TB
        C[CLOCK]
    end
    DP --> DS[DATA SELECTION]
    C --> DS
    DS --> TC[TRANSMISSION CIRCUIT]

```

FIG. 21

ALERT	SID	DID	DID	CP	DATA 0		TIME DATA	TIME DATA	CRC	CRC
(DATA N - 1) (DATA N)										

**FIG. 23**



**FIG. 23**

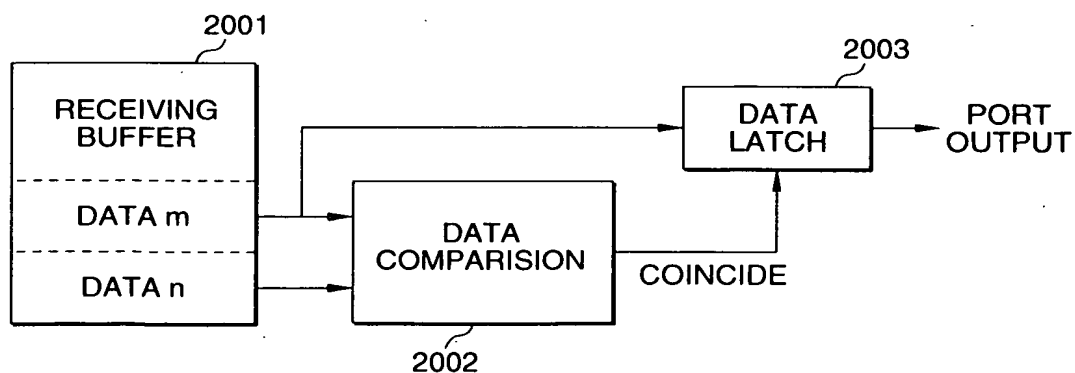
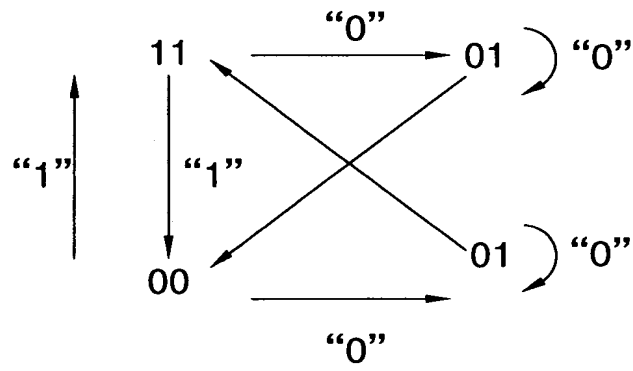


FIG. 25



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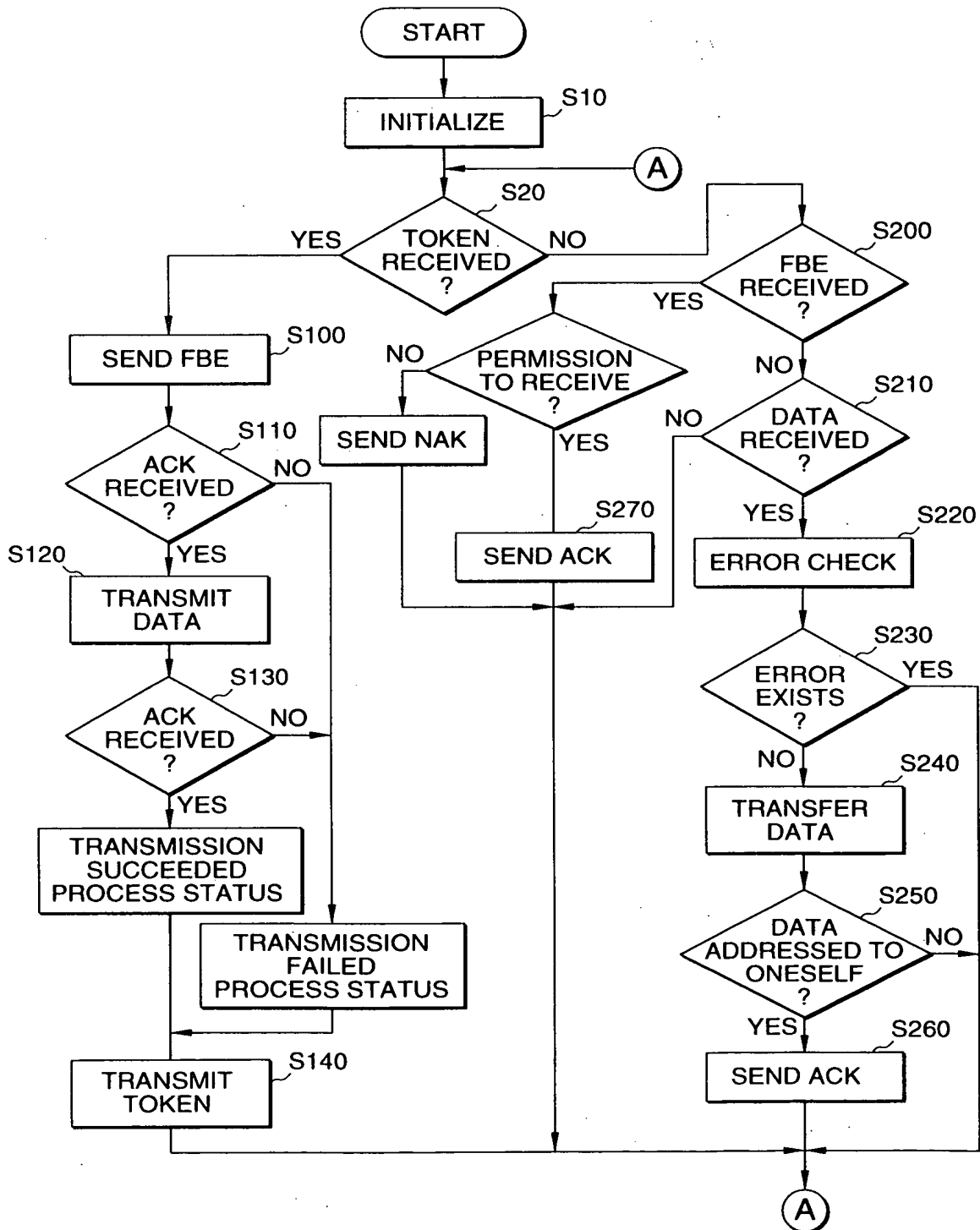


FIG. 27

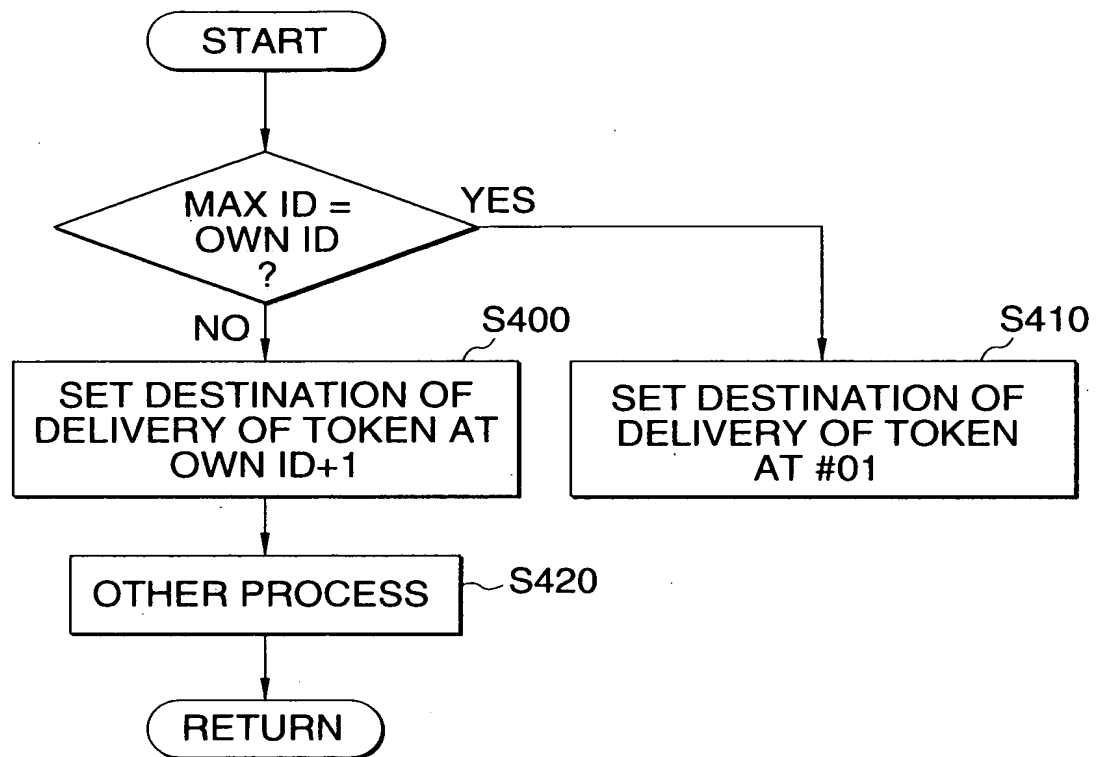


FIG. 28

